REMARKS

Claims 1-20 are pending; claims 1-6 are under examination, and claims 7-20 are withdrawn from consideration. Claim 1 is amended with this response. Reconsideration of the application in light of the following remarks is respectfully requested.

I. REJECTION OF CLAIMS 1-6 UNDER 35 U.S.C. § 103(a)

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,627,930 (Fox et al.) in view of U.S. Patent No. 6,831,313 (Uchiyama et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 1 has been amended to recite an integrated circuit, comprising an array of ferroelectric memory cells, wherein each cell has a capacitor stack having a ***single ferroelectric core layer*** with a ***crystallization in the (001) family***. ***At least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack***. At least one of the capacitor stacks comprises a conductive contact formed thereover or thereunder, or both. The conductive contact has a cross section near a contact portion with the top portion of the stack, the bottom portion of the stack, or both, that is about as large or larger than that of the ferroelectric cores.

Fox et al. do not teach such a **single ferroelectric core layer.** By contrast, Fox et al. teach a multi-layered cyrstallograpic textured structure, wherein the multiple "textures" describe multiple "crystal planes" (column 1, lines 60-61 of Fox et al.) of multiple ferroelectric layers, or a *first ferroelectric layer having a first crystallographic texture and a second ferroelectric layer having a second differing crystallographic texture* (Abstract, lines 6-10 of Fox et al.), and therefore the cited art does not teach this feature of the claimed invention.

Further, Fox et al. teach against the **single ferroelectric core layer** structure of claim 1 of the present invention, for example, stating that *the **multi-layered ferroelectric capacitors** disclosed provide much enhanced performance and operating*

characteristics over conventional ferroelectric devices incorporating dielectric layers having ***but a single crystallographic texture*** (a single Fe-layer) (Column 2, lines 59-63 of Fox et al.). Thus, one would not be motivated to combine the teaching of Fox et al. teaching ***multiple ferroelectric layers*** with Uchiyama et al. teaching a ***single homogenous ferroelectric core*** (Column 2, lines 18-22 of Uchiyama et al.) because such a modification would render the structure of Fox et al. unsatisfactory for it's intended purpose.

Fox et al. also discourage the <001> ***crystallization family*** orientation recited in claim 1, stating that growing ***ferroelectric dielectric layers having a <001> crystallographic texture*** *is generally* ***more difficult than growing*** *<111> or RND material,* which *is generally utilized* (Column 4, lines 17-21 of Fox et al.).

Finally, Fox et al. teach against the **single ferroelectric core layer** structure of claim 1 of the present invention, for example, teaching that *the* ***use of the added ferroelectric layer 24*** significantly reduces the undesired effects of dipole "pinning" which might otherwise occur when the bottom or top electrodes 12, 14 directly adjoin the ferroelectric bulk (core) (Column 2, lines 37-40 of Fox et al.). Thus, one would not be motivated to combine the above teachings of Fox et al. with Uchiyama et al. teaching a ***single homogenous ferroelectric core*** *material*, or a ***single composite material*** *comprising a ferroelectric component and a dielectric component* (Abstract, lines 3-6, and Column 2, lines 18-22 of Uchiyama et al.)

As highlighted above, the primary reference, Fox et al., do not teach the invention of independent claim 1, and one of ordinary skill in the art would not be motivated to combine with Uchiyama et al., or be motivated to modify the reference in accordance with Uchiyama et al. Therefore claims 2-6 are non-obvious over the cited art, and withdrawal of the rejections is therefore respectfully requested.

II. CONCLUSION

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36398.

Respectfully submitted,
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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: September 27, 2005

Christine Gillroy
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